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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 7,158,598	)	Serial No. 09/981,903
	)	
Inventor(s): Markus SCHETELIG et al.	)	Filed: October 19, 2001
	)	
Issue Date: January 2, 2007	)	Attorney Docket No. 006916.00009

For: METHOD AND DEVICE FOR IDENTIFYING A DATA PACKET IN A DATA STREAM

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves 1 page.

The mistakes identified in the appended Form occurred through no fault of the Applicants, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience is a copy of the Amendment filed February 3, 2006.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Since these changes are necessitated through no fault of the Applicants, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: May 10, 2007

By: _____
John M. Fleming
Reg. No. 56,536

Banner & Witcoff, Ltd
1100 13th Street, N.W., Suite 1200
Washington, D.C. 20005-4051
(202) 824-3000

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,158,598

DATED: January 2, 2007

INVENTOR(S): Markus SCHETELIG et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Claim 2, Column 10, Line 13:
Please delete "signal calculation" and insert --signal, calculation--

In Claim 14, Column 12, Line 18:
Please delete "voltage quotas and" and insert --voltage quota, and--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 7,158,598

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UNITED STATES PATENT AND TRADEMARK OFFICE

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DATED: January 2, 2007

INVENTOR(S): Markus SCHETELIG et al.

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Please delete "signal calculation" and insert --signal, calculation--

In Claim 14, Column 12, Line 18:
Please delete "voltage quotas and" and insert --voltage quota, and--

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FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 7,158,598

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MAY 15 2007

☒ PATENT ☐ DESI B&W Ref. 006916.0009 Da 2/3/06
☐ HAND CARRY Group Section ____ Bldg ____ Rm ____
Serial/Patent No. 09/981,903 Atty/Sec JMF/lls
Inventor Sheffield et al Client Baker et al.
Title Method and device for detecting a ...

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

☐ ____ total pp Spec., including : # of Claims ____
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☐ Sequence Listing - ☐ Diskette ☐ Paper
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PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	12

Application Number	09/981,903
Filing Date	10/19/2001
First Named Inventor	Markus Schetelig et al.
Art Unit	2638
Examiner Name	Kim, Kevin
Attorney Docket Number	006916.00009

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
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- ☐ Extension of Time Request
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- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
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Remarks

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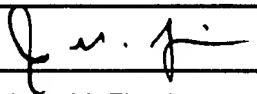
Signature			
Printed Name	John M. Fleming		
Date	02/03/2006	Reg. No.	56,536

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I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature			
Typed or printed name		Date	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Atty. Docket No.:	006916.00009
Markus Schetelig et al.			
Serial No.:	09/981,903	Group Art Unit:	2638
Filed:	October 19, 2001	Examiner:	Kim, Kevin
For:	Method and Device For Identifying A Data Packet in a Data Stream	Confirmation No.:	7306

RESPONSE AND AMENDMENT

U.S. Patent and Trademark Office
Customer Service Window Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the non-final Office Action mailed on November 10, 2005, Applicants respond as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-16 (canceled)

Claim 17 (currently amended): A method for identifying a data packet in a data stream in which

a d.c. voltage quota for a demodulated digital input signal is calculated in that the input signal is scanned in order to generate a sequence of scanned values ~~corresponding to the input signal~~ and from a selected number of the sequence of scanned values the d.c. voltage quota of the input signal is calculated;

a k-bit word is allocated to the input signal for that for each symbol of the input signal corresponding to a bit, a bit value is determined as a function of the d.c. voltage quota;

the k-bit word corresponding to the input signal is compared with an expected k-bit synchronization word in order to determine a correlation value; and

a packet identification signal is generated if the correlation value is greater than a correlation threshold value; and wherein

the d.c. voltage quota of the input signal is calculated again after each scan of the input signal at least until the correlation value determined by comparison of the k-bit word corresponding to the input signal with an expected k-bit synchronization word is greater than the correlation threshold value.

Claim 18 (currently amended): The method according to ~~Claim~~ claim 17, wherein after a packet identification signal has been generated, the corresponding correlation value is stored and scanning of the input signal, calculation of the d.c. voltage quota, and comparison of the k-bit word ~~corresponding to the input signal~~ with an expected k-bit synchronization word to determine the correlation value ~~is~~ are still continued for a predetermined period of time and a new packet identification signal is generated if a newly determined correlation value is greater than the correlation threshold value and greater than the previously determined stored correlation value.

Claim 19 (currently amended): The method according to claim 18, wherein to determine the k-bit word corresponding to the input signal, the input signal is scanned in order to generate a sequence of scanned values ~~corresponding to the input signal~~ and a bit value is allocated to each scanned value of a selected multiplicity of scanned values as a function of the d.c. voltage quota of the input signal.

Claim 20 (currently amended): The method according to claim 19, wherein the input signal is scanned at a frequency which is chosen in such a way that an ~~the~~ over-scanning rate is at least equal to two, that therefore at least two scanned values are determined for each symbol and to form the k-bit word corresponding to the input signal in each case only one scanned value per symbol is selected.

Claim 21 (currently amended): The method according to ~~Claim~~ claim 18, wherein the multiplicity of scanned values for forming the k-bit word corresponding to the input signal is selected from the sequence of scanned values in such a way that the selected scanned values within the sequence in each case are substantially the same distance apart.

Claim 22 (previously presented): The method according to claim 21, wherein the number of scanned values for calculating the d.c. voltage quota of the input signal is chosen in such a way that the scanned values correspond to areas in the expected k-bit synchronization word which substantially have the same number of bits with the value 0 and bits with the value 1 and the d.c. voltage quota is calculated as an average value of the scanned values.

Claim 23 (currently amended): The method according to ~~Claim~~ claim 22, wherein the number of scanned values for calculating the d.c. voltage quota consists of at least one group of scanned values in direct succession to one another, which correspond to successive symbols.

Claim 24 (currently amended): The method according to ~~Claim~~ claim 22, wherein the number of scanned values for calculating the d.c. voltage quota consists of two groups of scanned values, which are separated from one another by scanned values.

Claim 25 (currently amended): A device for identifying data packets in a data receiving stream with a delay line which has a number of storage places, in which scanned values of a demodulated digital input signal are stored in series, a d.c. voltage quota determining circuit, which is connected to the delay line in order to calculate a d.c. voltage quota of the input signal as an average value of a selected number of the scanned values comprising:

a decoding circuit connected to the delay line and the d.c. voltage quota determining circuit which compares a multiplicity of the scanned values with the d.c. voltage quota in order to allocate a bit value to each scanned value and in this way to form a k-bit word corresponding to the input signal;

a comparison and correlation calculating circuit which compares the k-bit word corresponding to the input signal with an expected k-bit synchronization word and calculates a correlation value for the k-bit word corresponding to the input signal; and

a correlation value comparison circuit which compares the correlation value supplied by the comparison and correlation calculating circuit with a correlation threshold value in order to supply a packet identification signal if the correlation value is greater than or equal to the correlation threshold value; and wherein

the decoding circuit comprises a multiplicity k of comparison circuits, to which in each case is applied the d.c. voltage quota and each of which is connected to one of the storage places of the delay line in order to compare the respective scanned value with the d.c. voltage quota and to determine a bit value, so the k-bit word corresponding to the input signal is applied to outputs of the decoding circuit.

Claim 26 (currently amended): The device according to ~~Claim~~ claim 25, wherein the number of storage places of the delay line corresponds to the number k of bits in the k-bit synchronization

word multiplied by ~~the~~ an over-scanning rate, in other words with the number of scanned values per symbol.

Claim 27 (currently amended): A device for identifying data packets in a data receiving stream with a delay line which has a number of storage places, in which scanned values of a demodulated digital input signal are stored in series, and a d.c. voltage quota determining circuit, which is connected to the delay line in order to calculate a d.c. voltage quota of the input signal as an average value of a selected number of the scanned values comprising:

a decoding circuit connected to the delay line and the d.c. voltage quota determining circuit which compares a multiplicity of the scanned values with the d.c. voltage quota in order to allocate a bit value to each scanned value and to form a k-bit word corresponding to the input signal;

a comparison and correlation calculating circuit which compares the k-bit word corresponding to the input signal with an expected k-bit synchronization word and calculates a correlation value for the k-bit word corresponding to the input signal; and

a correlation value comparison circuit which compares the correlation value supplied by the comparison and correlation calculating circuit with a correlation threshold value in order to supply a packet identification signal if the correlation value is greater than or equal to the correlation threshold value; and wherein

the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element;

one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line, which is separated from the first storage place by a multiplicity of storage places; and

the input, which is connected to the second storage place, is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein a sum supplied by the holding circuit is divided in the division circuit by a value corresponding to the distance between the storage places in order to calculate the d.c. voltage quota.

Claim 28 (currently amended): The device according to ~~Claim~~ claim 27, wherein two addition circuits connected to storage places of the delay line are provided, output signals of which are supplied to the division circuit via a further addition circuit.

Claim 29 (currently amended): The device according to ~~Claim~~ claim 28, wherein the comparison and correlation calculating circuit operatively connected to the decoding circuit, ~~and~~ a register storing the expected k-bit synchronization word, ~~besides~~ and a multiplicity k of comparison circuits for comparing the k-bit word ~~supplied by the decoding circuit and corresponding to the input signal~~ with the expected k-bit synchronization word, has a correlation element which adds a one for each coinciding bit pair in order to calculate the correlation value.

Claim 30 (currently amended): The method according ~~Claim~~ claim 17, wherein after a packet identification signal has been generated, the corresponding correlation value is stored and scanning of the input signal, calculation of the d.c. voltage quota, and comparison of the k-bit word corresponding to the input signal with an expected k-bit synchronization word to determine the correlation value ~~is~~ are still continued for a predeterminable period of time and a new packet identification signal is generated if a newly determined correlation value is greater than the correlation threshold value and greater than the previously determined stored correlation value.

Claim 31 (currently amended): The method according to ~~Claim~~ claim 23, wherein the number of scanned values for calculating the d.c. voltage quota consists of two groups of scanned values, which are separated from one another by a multiplicity of scanned values.

Claim 32 (currently amended): The device according to ~~Claim~~ claim 26, wherein the decoding circuit comprises a multiplicity k of comparison circuits, to which in each case is applied the d.c. voltage quota and each of which is connected to one of the storage places of the delay line in order to compare the respective scanned value with the d.c. voltage quota and to determine a bit

value, so a k-bit word corresponding to the input signal is applied to outputs of the decoding circuit.

Claim 33 (currently amended): The device according to ~~Claim~~ claim 26, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element, wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line which is separated from the first storage place by a multiplicity of storage places; and

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein the sum supplied by the holding circuit is divided in the division circuit by a value corresponding to the distance between the storage places in order to calculate the d.c. voltage quota.

Claim 34 (currently amended): The device according to ~~Claim~~ claim 25, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element, wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line which is separated from the first storage place by a multiplicity of storage places; and

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein a sum supplied by the holding circuit is divided in the division circuit by a value corresponding to the distance between the storage places in order to calculate the d.c. voltage quota.

Claim 35 (new): The method according to claim 22, wherein the number of scanned values for calculating the d.c. voltage quota includes at least one group of scanned values in direct succession to one another, which correspond to successive symbols.

Claim 36 (new): The method according to claim 25, wherein the number of scanned values for calculating the d.c. voltage quota includes two groups of scanned values, which are separated from one another by a multiplicity of scanned values.

Claim 37 (new): The method according to claim 22, wherein the number of scanned values for calculating the d.c. voltage quota includes two groups of scanned values, which are separated from one another by scanned values.

REMARKS/ARGUMENTS

The non-final Office Action of November 10, 2005 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 17-21, 23-34 have been amended. Claims 35-37 have been added. Claims 17-37 remain pending in this application.

Applicants thank the Examiner for the indication that claims 18 and 29 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112, second paragraph, and that claims 17-34 would be allowable if rewritten or amended to overcome the objections set forth in the Action..

Claim Objections

Claims 17-34 stand objected to due to alleged informalities. Without acquiescing to the objections, claims 17, 19, 20, and 26 have been amended to further clarify the scope of protection. Claims 18, 21, and 23-24, and 26-34 have also been amended to further clarify the scope of protection.

Claims 25 and 27 have not been amended to change the phrase "scanned values" to "the sequence of scanned values." The claims each recite that "scanned values of a demodulated digital input signal are stored in series." Antecedent basis for the phrase "scanned values" exists; therefore, Applicants contend that there is no need for amending to a "sequence of scanned values." Withdrawal of the objection of claims 25 and 27 is respectfully requested.

Rejections Under 35 U.S.C. § 112, second paragraph

Claims 18-24, 29, and 31 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter to which the Applicants regard as the invention. Applicants respectfully traverse this rejection.

Without acquiescing to the rejection, Applicants have amended dependent claim 18 to further clarify the scope of protection of the claim. The amendments are provided to clarify that scanning of the input signal is continued for a predetermined period of time, that calculation of the d.c. voltage quota is continued for a predetermined period of time, and that comparison of the

k-bit word with an expected k-bit synchronization word to determine the correlation value is continued for a predetermined period of time. Applicants believe the present rejection is mooted by the amendment made. Support for the amendment can be found throughout the original written description and drawings.

Without acquiescing to the rejection, Applicants have amended dependent claim 29 to further clarify the scope of protection of the claim. Claim 27, to which claim 29 depends on, recites "a decoding circuit...to form a k-bit word corresponding to the input signal." As such, Applicants have removed the phrase "supplied by the decoding circuit and corresponding to the input signal" as the phrase is redundant for identification of the k-bit word. Applicants have not amended the term "circuit" in line 2 of claim 2. The "comparison and correlation calculating circuit" is identified as such in Applicants' claim 27, to which claim 29 depends. Neither claim 27 nor claim 29 separately recites a "comparison circuit" and a "correlation circuit," as expressed in the Action. As such, amendment to "circuits" is not needed. Applicants believe the present rejection is mooted by the amendment made. Support for the amendment can be found throughout the original written description and drawings.

New claims 35-37 have been added to further clarify the scope of protection of the claims. Support for the claims can be found in Applicants' original written description and drawings. No new matter has been added with the respective new claims.

CONCLUSION

All objections and rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same. Should the Examiner find that a telephonic or personal interview would expedite passage to issue of the present application, the Examiner is encouraged to contact the undersigned attorney at the telephone number indicated below. If any additional required fees are or if an overpayment has been made the Commissioner is authorized to charge or credit Deposit Account No. 19-0733. Applicant looks forward to passage to issue of the present application at the earliest convenience of the Office.

Respectfully submitted,
BANNER & WITCOFF, LTD.

Date: February 3, 2006

By: _____
John M. Fleming
Registration No. 56,536

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